REMARKS

Claims 1-13 and 18-21 are pending in this Application, of which claims 1, 7, 12 and 18 are the independent claims. All claims stand rejected.

Claim 1 is being amended to correct an obvious drafting error, and is being amended to further clarify the scope of the claimed invention. In particular, amended Claim 1 recites: "row and column circuitry at each of the plurality of banks, the row and column circuitry configured to enable said writing other packet data to a respective bank independent of operation at other banks;" and "a plurality of multiplexers each associated with a different one of the segments of the serial registers, each multiplexer enabling said writing other packet data to the memory array from a respective segment of the serial register." Support for these amendments is found at least in Figs. 7 and 8 and on page 13, lines 1-22 of the Specification as originally filed. Claims 7, 12 and 18 are being amended in a similar manner. Acceptance is respectfully requested.

Claim 7 is being amended to further clarify the scope of the invention. Acceptance is respectfully requested.

Interview Summary

Applicant thanks Examiner for the helpful telephone interview conducted on June 11, 2009. Attending the interview were Examiner Hicham B. Foud and Attorney Benjamin J. Sparrow. During the interview, the rejections under 35 U.S.C. § 103 were discussed. Attorney Sparrow asserted that the Toda and Turner references do not make obvious the base claims because, contrary to the statements in the Office Action, Turner fails to teach or suggest the shortcomings of Toda that are stated in the Office Action. In particular, Turner does not teach "serial registers configured for receiving packet data from the associated input port at a segment of a serial register concurrent with writing other packet data to the memory array at another segment of the serial register," as recited in Claim 1.

Although no agreement was reached, it was also discussed whether the claims may be further clarified by reciting particular elements or operations associated with the serial registers. Accordingly, Applicant is amending claims 1, 7, 12 and 18 to further clarify the scope of the claims, and reconsideration is respectfully requested.

<u>Rejection of claims 1-13 and 18-21 under 35 U.S.C. § 103</u>

Claims 1, 2, 6, 7, 11-13, 18 and 21 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Toda et al. (U.S. Patent No. 5,612,925) in view of Turner (U.S. Patent No. 5,475,680). Claims 3-5, 8-10, 19 and 20 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Toda in view of Turner and further in view of Zuravleff et al. (U.S. Patent No. 5,867,735). Applicants respectfully disagree with these rejections in view of the claims as currently amended, and reconsideration is respectfully requested.

Amended Claim 1 is directed to a packet buffer random access memory (PBRAM) device. Without limitation of the claims, an example PBRAM device is illustrated in Fig. 7, where the PBRAM device 62 includes a memory array 74 having 8x8 memory banks, a plurality of input ports 70 (I/O Port 0 – I/O Port 31), and a plurality of serial registers 72 associated with the input ports 70 (serial register 0 – serial register 31). The serial registers 72 each receive packet data from one of the associated ports 70 and write the packet data to the memory array 74 (see Specification, page 4, lines 3-11). Each of the serial registers 72 is further segmented into a plurality of segments, each segment being associated with corresponding portions of the memory array 74. Such a configuration is illustrated in Fig. 8, where a serial register 72 is divided into segments of 256 bits each. Further, a segment of the serial register 72 may transfer data into the memory 74 concurrent with another segment of the serial register 72 receiving other data (page 13, lines 11-15). A plurality of multiplexers 76, each associated with a different segment of the serial register 72, enables this transfer from the segment, independent of other segments, to an address of the memory 74 (page 13, lines 5-8). Further, each bank of the memory array 74 includes row and column circuitry to select the address to receive the packet data independent of operation at other banks (page 13, lines 1-5). As a result, the packet data can be transferred from one segment of the serial register to a selected data bank, while another segment of the serial register receives other data concurrently.

Toda discloses a memory device for transferring data to and from a memory. As shown in Fig. 16, the memory device 161 includes a memory cell 162, a serial register 167 (the label "164" is a typographical error; see col. 12, lines 25-28), and a data I/O port 164. The serial register 167 has 8 bits. During a typical write operation, data received at the I/O port is

transferred serially into the serial register 167. Once an address of the memory cell 162 is selected, the serial register 167 transfers the 8 data bits simultaneously into the memory cell at the selected address (col. 12, lines 17-33).

Toda fails to disclose "a plurality of input ports," where a "memory array…[is] shared by the plurality of input ports," as recited in Claim 1. As shown in Fig. 16, Toda discloses only a single I/O port 164, and does not teach or suggest additional ports for storing data to the memory cell 162. Toda's failure to teach "a plurality of input ports" was pointed out in two previous Amendments (*see* Amendment filed June 28, 2007, pages 9-10; and Amendment filed December 3, 2007, page 8). As a result of Applicant's previous remarks, a § 102 rejection of Claim 1 with regard to Toda was withdrawn, and a subsequent Office Action relied instead on Joffe (U.S. Patent No. 5,440,523) for the teaching of "a plurality of input ports" (*see* Office Action mailed February 5, 2008, page 3). Though Joffe is no longer relied upon, Toda still fails to disclose or suggest "a plurality of input ports" as recited in Claim 1.

The Office Action states that Toda fails to disclose 1) "a plurality of serial registers each associated with a different one of the plurality of input ports," and 2) "each of the serial registers [being] configured for receiving packet data from the associated input port at a segment of a serial register concurrent with writing other packet data to the memory array at another segment of the serial register," as recited in Claim 1. Applicant agrees. However, Turner, on which the Examiner relies for those features, also fails to suggest at least some of the aforementioned features.

Turner discloses an asynchronous time division multiplex (ATDM) switching system. As shown in Fig. 4, Turner receives data packets via 16 serial input lines 107 to a serial-to-parallel converter 100. The converter 100 includes two shift registers for each input line, where each shift register stores one half of a packet received at the respective input line (col. 3, line 58 – col. 4, line 8). These two packet halves, referred to as "A halves" and "B halves," are then transferred from the shift registers into separate blocks of RAM, "A Data" RAM 101 and "B Data" RAM 102, respectively (col. 4, lines 5-15).

Turner fails to disclose "serial registers configured for receiving packet data from the associated port at a segment of a serial register concurrent with writing other packet data to the memory array from another segment of the serial register" as recited in amended Claim 1.

Turner does state that one register (e.g., the "A data" register) can transfer data to a respective RAM block at the same time that another register (e.g., the "B data" register) is loaded with data from the input port (col. 4, lines 8-15). Turner does not teach or suggest configuring either an "A data" or "B data" register for receiving packet data to one segment of a register concurrently with writing other packet data from another segment of the register.

Further, Turner does not teach "row and column circuitry at each of the plurality of banks" as now recited in amended Claim 1. As shown in Fig. 4, Turner uses a demultiplexer to direct packet data to each of the data banks 101, 102. Because the demultiplexer selects among the data banks 101, 102, only one data bank requires row and column circuitry to receive data at a given time. Thus, Turner's system does not suggest "row and column circuitry" at each of the banks, and instead uses a single controller (queue processor 104) to control each of the data banks 101, 102.

Turner also does not teach "a plurality of multiplexers each associated with a different one of the segments of the serial registers" as now recited in amended Claim 1. As described above, Turner uses a single demultiplexer to transfer data from all of the shift registers 100. Turner provides no teaching or suggestion of a multiplexer for each segment of a register, and does not suggest a need for such a configuration because the queue processor 104 instead determines the location where each packet will be written in the data banks 101, 102 (col. 4, lines 11-16).

For at least the reasons above, Turner fails to disclose the "serial registers" as recited in Claim 1. Accordingly, even a combination of the references does not teach all elements of the claims.

Amended Claim 7 and Claims 12 and 18 recite features comparable to those described above with respect to Claim 1, and so are not anticipated nor made obvious by Toda and Turner. Claims 2, 6, 11, 13 and 21 depend from one of claims 1, 7, 12 and 18 and so inherit the features described above. Due to the aforementioned shortcomings of Toda and Turner, no combination of Toda, Turner and Zuravleff render obvious the invention as recited in Claims 3-5, 8-10, 19 and 20. As a result, the § 103 rejection of Claims 1-13 and 18-21 is believed to be overcome, and reconsideration is respectfully requested.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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